Status and future of HDI PWBs

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Abstract

Higher packaging density for the next generation of electronic devices require the utilization of inner space of a PWB for component placement. This will shift some added value assembly processes from the assembly houses backwards to the PWB fabricator. (Regardless whether it is liked or dislike by the PWB fabricators).
ASPOCOMP as a leader in advanced PWB technology is developing this technologies to meet the needs of key OEMs.
The paper will describe what the present experience with this new technology will be and where the technology limits are. Material supplies will be challenged to come up with better solutions as they exist today. Sequential versus parallel PWB manufacturing processes will be reviewed and what is needed to meet the manufacturing and cost target for the next generation of PWBs.

PWB product trends and background

A key to the success of Aspocomp over the years has been its focus on high density interconnects (HDIs) for mobile telephones, base station PWBs and on specific high value-added PWBs for automotive, industrial electronic and other applications. Since the company has several factories in different parts of the world, each factory is focused on their particular market segments, and on advanced technology, with co-ordination of centralized technology management. To meet the challenges of the market-place, process automation has been an important factor in remaining competitive.

Close co-operation with key customers and suppliers was needed to understand the future road maps and requirements. We, as PWB fabricators, had to recommend the best technical and most cost-effective manufacturing technology to our customers' designers. This resulted in a 'design for manufacturing' approach, providing technical solutions for the OEMs, EMSs and cost-effective fabrication at our factory. This also helped with the selection of the most appropriate and correct investment in new technology.

Trends of electronic devices have requirements for higher frequency, more functionality and miniaturization. More active and passive components are needed and less surface is space available. So embedding components in the PWB is an ongoing development project. This new technology will also give new requirements for the materials used in the HDI board. The dielectric material has to be more stabile during PWB production and all the material properties have to have tighter tolerances. Advanced materials were also required to help meet the challenges posed by the OEMs' future needs. These materials range from:

- resin coated copper foil (RCF) or pure resin
- thin glass layers FR-4 or special LD glass
- aramid-reinforced microvia layers.
- PTFE reinforced mircovia layers

New lamination processing technology was equally needed to reduce the thickness tolerances of the dielectric material inside the multilayer so as to meet the electrical and impedance requirements of advanced

electronic equipment. It also gives the possibility to new dielectric application process like liquid lamination of dielectric.

Aspocomp has, since 1995, been one of the pioneers in using induction-heated multilayer pressing technology called Adara press. This was needed to enlarge the processing window for a wide range of resin and reinforcement technologies used at the company's different factories.

Production experience

In this section, some of the key steps are reported. It must be understood that we can only report on our own particular findings and that experience has to be gained on an individual basis by different production units. Similarities may be noticed with other factories, but many process steps are dependent on the equipment, chemicals and the production experience of the people involved in the fabrication process. This is not, therefore, a process guide, but rather a report on a few specific items that are important for designers who have to make decisions but who are not directly involved in the day-to-day business of manufacturing PWBs.

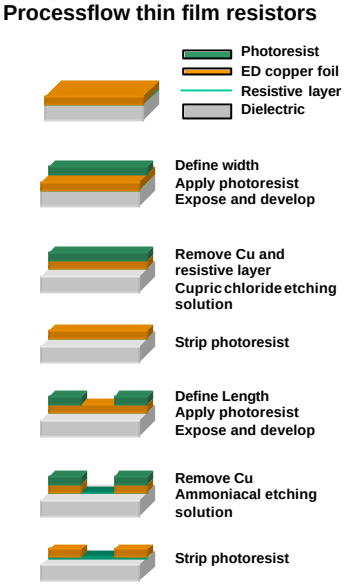
Embedded components, resistors

To meet the requirements in the wireless communication for high frequency, high volume and low production cost, we have started the evaluation of integrating the passive components in to the PWB board. Advantages of using embedded resistors are to reduce cost, save PWB surface space for more valuable components, improve reliability by eliminating solder joints, possibility to reduce size of the PWB and improve performance by reducing inductance loops. The high level of interest is primarily focused on resistors and capacitors since they present the majority of passive components used in the PWB.

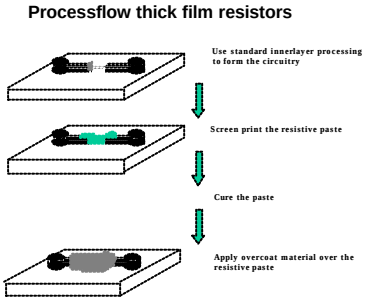
There are mainly three different technologies available for embedding the resistors; these are thin film, thick film or plating technology. At least Ohmega, Gould, Shipley and Mitsui are offering the thin film resistor material. Thick film materials supplier are DuPont and Asahi. The plating resistor process has been evaluated with MacDermid. All these technologies have their advantages. Our goal for the project is to find out the best available technology for volume production by utilizing the existing machinery and processes as much as possible.

Thin film technology generally refers to thin coatings like 100 to 1000 Ångströms coated by sputtering to copper foil surface. Typically used nickel alloys. The sputtering technique gives consistent and uniform coating of the resistive layer on copper foil. The tolerance of the coating is important when discussing of the final tolerance of the embedded resistors on PWB. Looking from the processing point the thin film technology needs more innerlayer capacity and also an extra etching process for the resistor layer. The learning curve for imaging and etching steps has to be studied, to be able to keep the tolerance of the resistor. We have found out that with thin film technology we can produce the resistors with ? 5% tolerance in final PWB. If customers' requirement for the tolerance is tighter, the trimming is needed and then we can trim the resistors and also apply the testing simultaneously. By trimming the resistor values can only be increased, because trimming in based on material laser cutting. The disadvantage of the thin film is that you have to use the same sheet resistance (? /sq) all over the layer. Large variety of the resistors simultaneously on the same PWB layer with one sheet resistance is difficult or impossible to design or at least you will loose the space benefit. The designer has to understand in which layer of the PWB the resistor can be build. The resistor layers should be in the inner

layer core so that the imaging and etching processes can be done accurately.



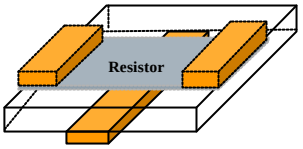
Figur 1: Process flow for embedded resistor with thin film technology [2]



Figur 2: Process flow for embedded resistor with thick film technology

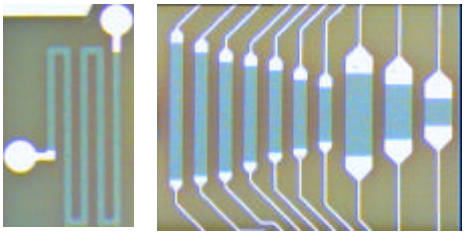
Thick film technology needs some capable screen-printing machine to meet the accuracy and registration requirement. Also the curing of the thick film paste needs some equipments, which might be from the standard heat-curing oven at 150C to high temperature furnace at 900C. Tolerances achieved are typically ± 20%, so the trimming will be obvious process step. These could be trimmed to tolerance range of ± 1%.

The embedded passives are placed between the dielectric materials. So the PWB designer has to be a part of the project in very early stage. It is important to understand in which layers the resistors can be embedded without extra processing steps. Also the behavior of the dielectric materials must be known because all tolerances are more critical. The mechanical properties of the dielectric materials are important when processing the embedded resistor, so that no cracks are created during the processing of the PWB.



Figur 3: No resistor cracks under stress conditions are allowed

During the project we have found out that the infrastructure for the embedded components and their design is not fully covered and understood. We have worked very closely with the design tool, AOI, electrical test and trimming companies to find out the best solutions for the embedded resistor production. For example the PWB CAD softwares are not well equipped to deal with embedded passives on innerlayers and simulation and modelling software is not available although currently under development. This lack of design rules results longer turnaround, because the whole innerlayer must be redesigned with manual operation.



Figur 4: Different resistor lay-outs

Base material selection

It has become an established standard that the core of a HDI PWB is made of FR4 glass-reinforced laminate. This material is well known and has been tested and accepted as meeting most of the standards required for PWBs. The material has been used in this application for a number of years and

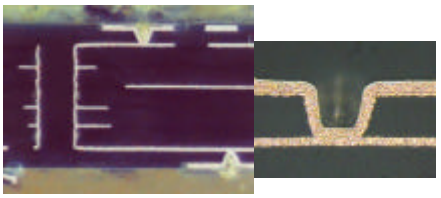
most fabricators and OEMs are familiar with its use.

Microvia technology, on the other hand, is a relatively new technology, so PWB designers and fabricators, and assembly houses, considering its adoption are more open to innovation and to the use of a wider range of materials.

Materials for microvia layers
A number of different reinforced and non-reinforced materials are available for microvia applications. However, before selecting any particular alternative, it is vital to define the needs of the OEMs and designers, so that a correct choice can be made. In this next section, the key features of the most important materials for microvias will be reviewed.

Resin Coated Foil (RCF)
Resin coated foil is the material that is most widely used today for the microvia layer. Being a pure resin system, it offers all the advantages of a resin system, as well as the disadvantages of pure resin. As the RCF is not reinforced with any glass or organic material, its chief characteristics and virtues are:

- fast laser hole formation (relative)
- suitable processing in standard PWB processes
- multiple suppliers
- new modifications of the resin can be used to make the RCF processing easier and the end product more reliable and halogen free (like adding some fillers)
- at 1 GHz , RCF has a lower Dielectric Constant (Dk) 3,4 than FR4, which has a Dk of 4.2 ± 0,3, depending on the resin content
- good flow and hole-filling properties for small holes with a diameter of up to 0.2 mm and with board thickness of 1,0 mm without separate hole plugging process
- a maximum dielectric thickness of 70 µm of the finished PWB (max 100 µm resin at B stage). If there are many holes in the board, it is difficult to achieve this dielectric thickness, as resin may flow into the holes, resulting in reduced thickness and larger tolerances
- dielectric thickness tolerances often ± 20 µm, depending on the RCF thickness and design of the PWB like ground/signal copper layer lay-out, copper plating thickness and the resin thickness used. If the outer layers of the FR4 core board are made using the standard pattern plating process, the Cu plating thickness on the outer area of a panel can vary. Cu panel plating of the core outer layers may offer a more even thickness of the copper and thus smaller tolerances
- when resins are used as a dielectric layer in HDI boards, they have a high coefficient of thermal expansion (CTE). This could be a risk for the cracks after thermal shock specially when big and heavy fine pitch components are used, also new types of resins are developed to meet the mechanical requirement.
- the high CTE increases the stress on the solder joints. In conjunction with lead-free solder, this could lead to failure of electronic equipment in the field. So new modified epoxies are needed.

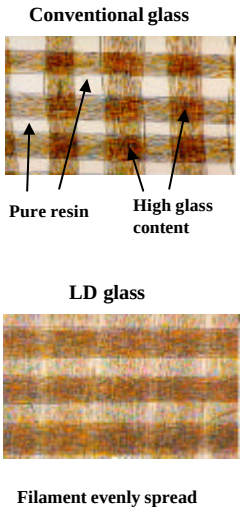


Figur 5 : Shows examples of the RCF board with buried core

Thin glass-reinforced material for microvia-layers
Prepregs with a 2114, 1080 or 106 glass cloth have been tried for use as the microvia layer, although we have not used this material for any volume application in our factories. The main reason for this is that the woven structure has large openings and the fibre weaves create a thick fibreglass

bundle. The filaments on the FR4 glass-cloths are from 5 to 9 µm. It seems to be so that this also has an influence for the laser via formation capability. The filaments on 106 and 1080 prepregs are 5 µm and on the 2114 they are 7 µm. We also found out that hole wall surface texture is relatively rough. This is a fundamental fact because the ablation threshold is higher to the glass than to the epoxy. This unevenness may disturb the plating process, leading to variations of the laser drilled hole shape and diameter as well as uneven plating.

New LD or random type glass-reinforced prepregs are now offered by several suppliers. LD series available with 106 and 1080 compatible glass fabric. On these materials the yarn on the glass-cloth is not twisted or the twisting has been reduced. These materials give more stabile distribution of the filaments on the glass-cloth so capability for laser has been improved. Tests of these materials are ongoing and it looks a possible alternative to RCF.

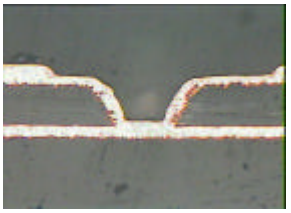


Figur 6. Different glass clothes [1]

The key characteristics of the material are:

- using prepreg 1080 (normal glass fibre) the thickness tolerances with 65 ± 25 µm with all lay-out designs can be achieved.
- the microvia holes size is depending on the used prepreg type and is normally bigger than with RCF
- the coefficient of thermal expansion is similar to glass-reinforced FR4 with a CTE of 14 to 18 ppm/°C (with copper), depending on the resin content and copper thickness. This is an improvement over RCF which has a CTE of up to 60 ppm/°C
- the Dielectric Constant (Dk) of the material is 4.2 ± 0,3, depending on resin content. This is due to the fact that the Dk of glass is 6.2 and 3.6 for resin

It should be noted, however, that, since this material has not been on the market for very long, more production experience is needed to secure whether it is a valuable, and viable, alternative for RCF.



Figur 7: Laser drilled prepreg 1080

The increasing demand for higher packaging density is simultaneously increasing the risk for the conductive anodic filaments (CAF) seen already in the plated through holes. These false connections grow with conductive ions along the filaments when current is present or at increased temperature/humidity with small currents. So this has to be kept in mind when working with glass fiber prepreg designs. Especially this is the case when the plated through holes and/or the micro via holes are very near each other e.g. under high I/O count CSP component. The test conditions used for CAF is following 85% RH/85C/50 V DC. The new types of dielectric materials are developed to avoid this phenomenon.

Aramid (Thermount ®) laminate and prepreg

During the course of the last 4 years, Aspocomp has manufactured a wide range of PWBs using Aramid (Thermount®) laminate and prepreg. Printed wiring boards containing this laminate and prepreg are now available as standard products from Aspocomp, along with PWBs made with resin coated foil.

During the period when we were evaluating and introducing the aramid-reinforced PWBs, we had to learn how to deal with an entirely different reinforcement material made from a very strong organic fibre. We also had to learn a different routing process to control the outside shape of the PWB assembly arrays.

Essentially, Thermount® laminates and prepregs have the following characteristics:

- As a laminate, the aramid will have a Dk of less then 4.0 (the aramid fibre has a Dielectric Constant (Dk) of 4.1), depending on the resin content
- laser drilling is very similar to that for RCF
- the material is supplied from all licensed laminators with high Tg resin systems
- it is supplied as a laminate or as a prepreg
- the thickness of the dielectric material can be selected depending on the needs of our customers
- the dielectric thickness can vary from less than 40 µm (under a test programme) to 50 µm, 75 µm and 100 µm. For special applications, a thickness of 150 µm can be used
- the aramid has excellent dimensional consistency, making possible small annular rings around the through- and microvia holes. Using the optimal multilayer pressing process we can achieve good registration in the big production panel size
- due to the organic fibre in the material, the routing conditions in the process need to be modified.

One of the biggest issues that we had to overcome was the perception that aramids absorb a lot of moisture and will, as a result, delaminate during the soldering operation.

When we first started working with this material, we also came across delamination. Believing that this was due to moisture, we introduced a thermal baking process to solve the moisture problem. However the problem surfaced again and we could not understand where the humidity was coming from.

So, detailed studies were carried out with different resin systems, and the organic reinforcement from DuPont, to optimise the pressing cycle in the multilayer press. It was discovered that the delamination phenomenon was caused by insufficiently cured epoxy resin. Since the epoxy resin in the Thermount® laminate and prepreg is a material with a high Tg, longer pressing cycles are required. The heat transfer rate of the aramid is also slower compared to glass. This was another factor that we had to understand, and take into account, when we were setting up the pressing cycle.

In the beginning of the project the peel strength was as low as 0,9 to 1,0 kN/m with aramid materials. This issue was studied together with the laminate and copper foil suppliers. Choosing the right resin system and optimized copper foil treatment for the aramid construction the peel strength problem was solved.

PTFE reinforced materials

We have tested the Microlam 600 material from Gore, which is dielectric consisting of FR-4 epoxy resin reinforced with non-woven teflon. This material is targeted to applications with 1 or 2 micro via layers per side.

- laser drilling similar to RCF
- thin and homogeneous material (9 to 90 micron thick)
- stable electrical properties from 1 MHz to 10 Ghz: Dk 3,0 and loss tangent 0,017 at 3 GHz
- CTE value same as RCF 60 ppm/C
- low cured modulus for reduced substrate stress

Pressing of multilayers using induction-heated presses, Adara press

Nearly 6 years ago, Aspocomp decided that induction-heated Adara presses would fit for the production process better than standard oil-heated presses. In an extensive test program, the heat distribution and tolerance requirements were evaluated. Our experience after many years of operation is that this press enables us to:

- press multilayers with highly accurate thickness tolerances
- cure the resin as required by the laminate suppliers
- have an even heat distribution over the full panel
- press up to 70 panels in one book resulting in high productivity, and
- use minimum energy.

This pressing technology gives also benefit when we started the embedded component project. This very flexible pressing technique gives the possibility to make the different resistor applications in our big production panel with good through put. The registration is one of the critical parameter also in the resistor application.

Figur 8: Adara presses in Salo factory

Cost-reduction requirements

The reduction in the pitch size of the chip scale package means that 2 or even 3 microvia layers are needed on each side of the PWB.

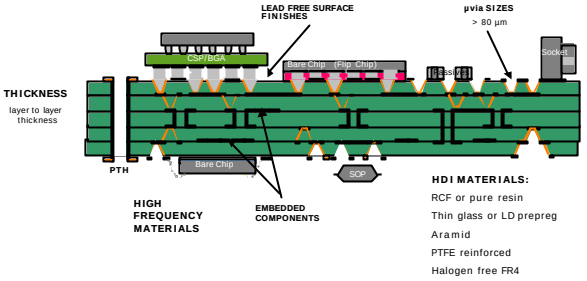


Figure 9. A schematic of the near future technology PWB, which offers the opportunity to reduce the cost, save valuable PWB surface space, improve reliability by eliminating solder joints and improve performance by reducing inductance loops.

There are different possibilities to make the build up of the final PWB. You can use e.g. core gap technology, which can be made with short process flow. But it might require larger microvia holes and this may not be possible in all cases. However, in order to lower the cost of electronic equipment, designers may consider what technology to use to obtain the cost benefits of a different production processes. In our role as PWB fabricators, we have to involve the whole supply chain to ensure that the electronic equipment meets the technical, performance and cost expectations of the end-user.

Summary

Microvia technology has changed the way how PWBs are made and how circuit miniaturisation will continue. The next task is to introduce the embedded components as a reliable and competitive added value technology for PWBs. The challenge we must face is to remain at the forefront of technology. Since we are in the business of manufacturing PWBs for world markets, we should be open minded for new technologies. Close and effective co-operation with all business partners, and even sometimes with competitors, will help us to move ahead and keep abreast of advances in technology.

This paper has been presented in IEEE Conference in Atlanta 6.3.2002

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