Description of Conductive Anodic Filament Test Vehicle #1, i.e., CAF TV1

by Michael Freda, Sun Microsystems Inc.

Introduction

It is Sun Microsystems' (Sun's) opinion that modern PCB fab (i.e., printed wiring boards) designs with ever decreasing dielectric spacings are approaching the limits of long term reliability for traditional FR4 epoxy/glass material using current industry accepted processing methods. To continue to shrink non common conductors ever closer it is probable that new or improved materials will need to be used and/or developed so that reliability is not compromised. Sun feels that testing using temperature, humidity, and bias test methods to accelerate the formation of conductive filaments is an appropriate test method for evaluating long term reliability.

The majority of research done in this area was conducted in the late 70's and early 80's by Bell Laboratories[1, 2 & 3]. Subsequent work in this field has also been performed by the University of Maryland (CALCE) and by the Georgia Institute of Technology. The work done by Bell Labs provides a good understanding of the basic two step mechanism involved, acceleration models for temperature, humidity, bias, and, a ranking of material performance for different resin and reinforcement combinations. Unfortunately, the dielectric spacing used in the Bell Labs testing was much larger than what is commonly used today. There are also questions about the performance of materials used today: Are some of the new resins and reinforcements used today better? Have some of the old materials improved?

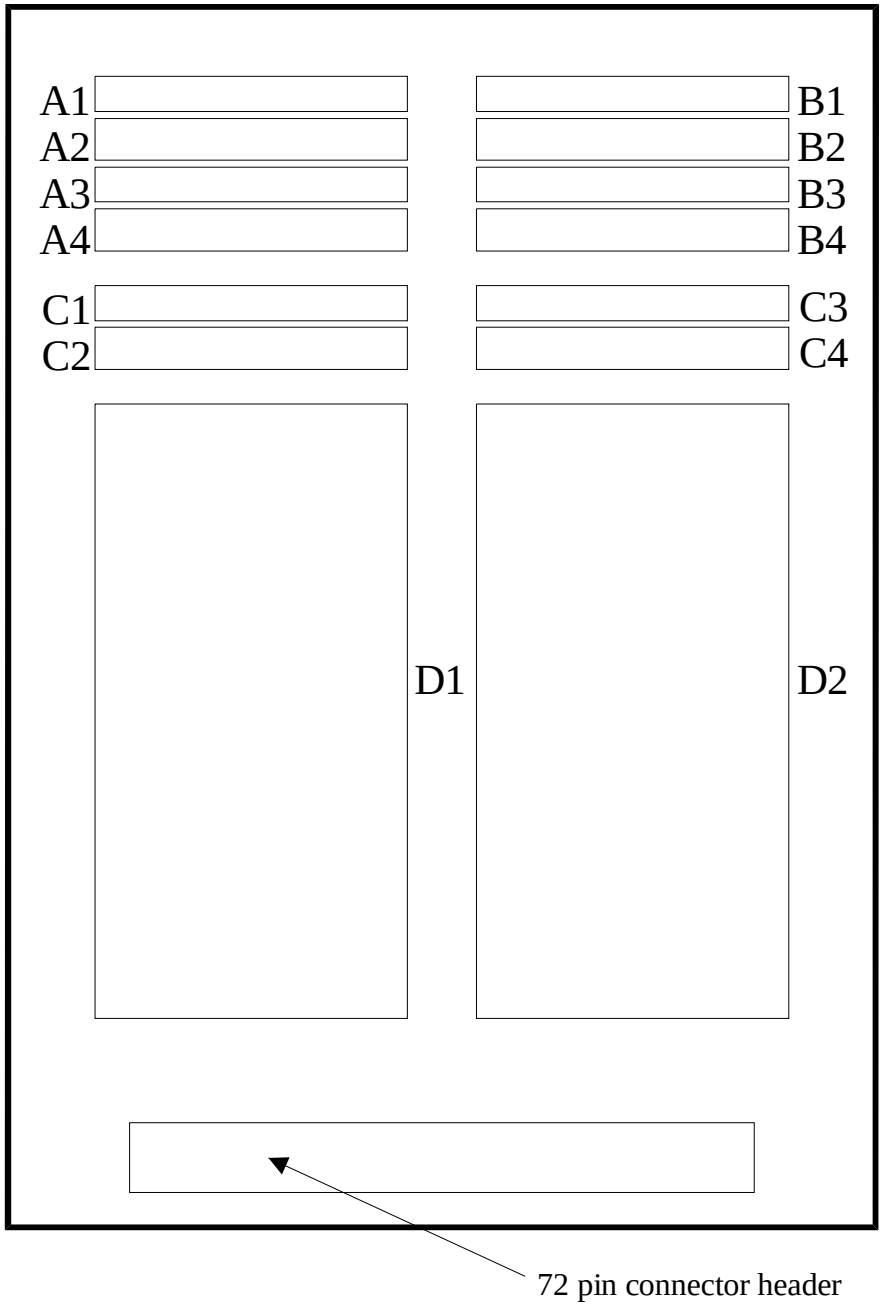
To answer some of these questions, conductive anodic filament test vehicle one (CAF TV1) was designed by Sun for CAF testing. The Bell Labs CAF test board used vias on a fixed grid with alternating vias having a positive or negative bias. The Sun designed CAF TV1 is a 10 layer, 5 x 7 inch PCB fab which has four types of test structures:

1) via to via like Bell Labs with vias in line with woven glass fibers, four via to via spacings are used
2) via to via with vias at a 45° angle to the woven glass fibers, four via to via spacings are used
3) via to antipad, four via to inner layer antipad spacings are used
4) layer to layer.

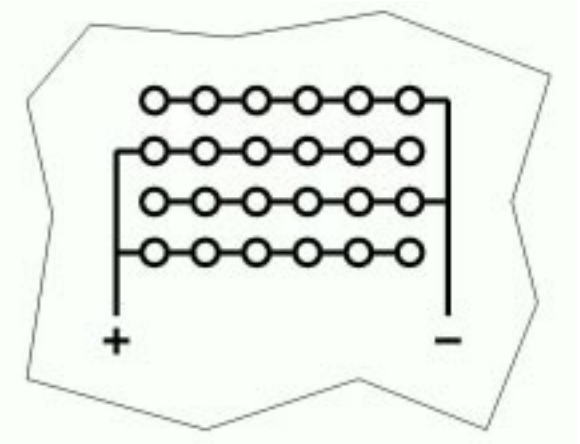
These structure cover the three types of shorting paths that could occur in a standard PCB fab design. Additionally, in the first three structures, the spacing from the positive to the negative electrodes is varied in four steps from commonly used spacings to very aggressive spacings. The test structures are described in more detail in the sections which follow.

CAF TV1 Board Layout

The layout of the test structures on the CAF TV1 PCB fab is shown below. The board is 5 x 7 inch. The pages which follow provide details on each of the test structures.



Test Structures A1 through A4



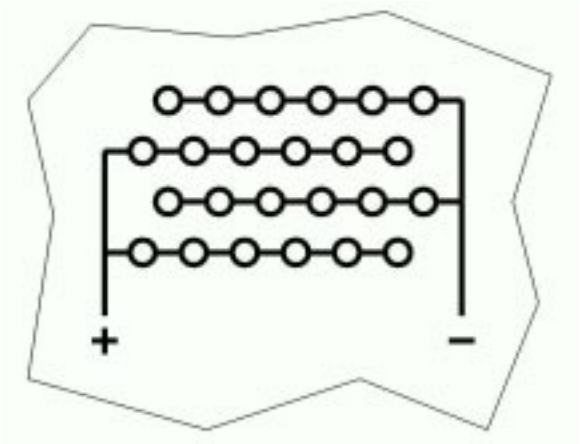
The four "A" test structures have 5 alternating rows of vias. Within each structure, each row has 42 vias with alternating rows being tied to positive or negative electrodes. The via edge to via edge spacing is varied from one structure to the next by using a different drilled hole size on the same 40 x 40 mil via grid. The resulting via edge to via edge spacings are: 10.8, 15, 20 and 25.5 mils. Other than the use of different drilled hole sizes and a small change in pad sizes, the four structures are identical. The vias in the "A" test structure are aligned with the glass fibers. Within a given test structure, the inner and outer layer pads for all ten layers are the same, i.e., the same pad size is consistently used within a given test structure although, it does change from stucture to structure. All via to electrode connections are made on layer 1 and are repeated on layer 10 so that a single etchout will not effect results.

A conceptual representation of the "A" test structure is shown to the upper right. Design details on each of the four "A" test structures follows in Table 1.

Table 1 − Test Structures A1 through A4 Design Rules

	A1	***A2***	***A3***	***A4***
Outer layer pad size	34 mil	32 mil	30 mil	27 mil
Inner layer pad size	34 mil	32 mil	30 mil	27 mil
Drilled hole size	29.2 mil	25 mil	20 mil	14.5 mil
Via edge to via edge (shortest distance)	10.8 mil	15 mil	20 mil	25.5 mil
Via edge to via edge (Manhattan distance)	10.8 mil	15 mil	20 mil	25.5 mil
Bias pins	1 to 5	2 to 5	3 to 5	4 to 5

Test Structures B1 through B4



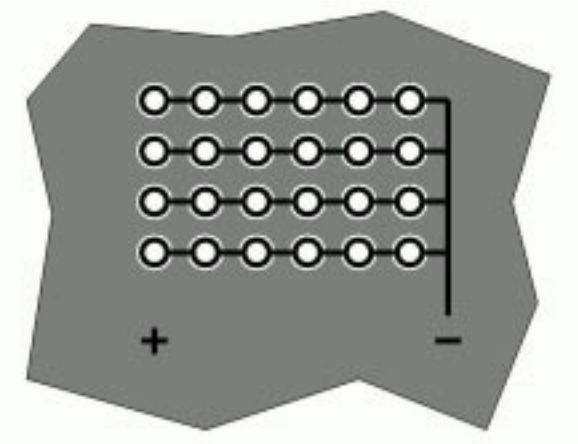
The four "B" test structures have 7 alternating rows of vias. Within each structure, alternating rows have either 27 or 26 vias with the alternating rows being tied to either positive or negative electrodes. The via edge to via edge spacing is varied from one structure to the next by using a different drilled hole size on the same 60 x 60 mil via grid. The 60 x 60 mil grid has an interstitial via therefore, tipping at a 45° angle results in a square 42.4 x 42.4 mil grid.Note: the sketch does not look square when tipped 45° but, the CAF TV1 fabs do. The resulting via edge to via edge spacings are: 10.4, 14.4, 19.9 and 24.4 mils. Other than the use of different drilled hole sizes and a small change in pad sizes, the four structures are identical. The vias in the "B" test structure are **not** aligned with the glass fibers. If the failure mode is along glass bundles it is reasonable to expect the "B" test structure to perform better than the "A" structure for equivalent via edge to via edge spacings. Within a given test structure, the inner and outer layer pads for all ten layers are the same, i.e., the same pad size is consistently used within a given test structure although, it does change from stucture to structure. All via to electrode connections are made on layer 1 and are repeated on layer 10 so that a single etchout will not effect results.

A conceptual representation of the "B" test structure is shown to the upper right. Design details on each of the four "B" test structures follows in Table 2.

Table 2 − Test Structures B1 through B4 Design Rules

	B1	***B2***	***B3***	***B4***
Outer layer pad size	37 mil	35 mil	33 mil	30 mil
Inner layer pad size	37 mil	35 mil	33 mil	30 mil
Drilled hole size	32 mil	28 mil	22.5 mil	18 mil
Via edge to via edge (shortest distance)	10.4 mil	14.4 mil	19.9 mil	24.4 mil
Via edge to via edge (Manhattan distance)	14.75 mil	20.4 mil	28.2 mil	34.55 mil
Bias pins	7 to 11	8 to 11	9 to 11	10 to 11

Test Structures C1 through C4



The four "C" test structures have 5 rows of vias with each row having 42 vias. All 5 rows of vias are electrically tied together to form one electrode with inner layer planes on layers 2 through 9 forming the other electrode. The via edge to inner layer antipad edge spacing is varied from one structure to the next by using a common drilled hole size and varying the opening of the antipad clearance. The same 40 x 40 mil via grid used in "A" is used in "B". The resulting via edge to inner layer antipad edge spacings are: 10.5, 13.5, 18.5, and 23.5 mils. This spacing assumes optimum registration which is impossible but, the CAF TV1 design leaves adequate room to place an onboard PerfecTest coupon. Other than the use of different anitpad clearances the four structures are identical. The vias in this test structure are aligned with the glass fibers the same as the "A" structures. All four test structure use the same drilled hole size and the same outer layer pad diameter. All via to via electrode connections are made on layer 1 and are repeated on layer 10 so that a single etchout will not effect results.

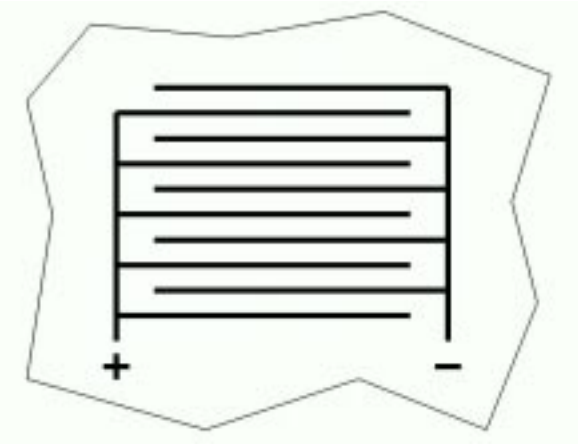
A conceptual representation of the "C" test structure is shown to the upper right. Design details on each of the four "C" test structures follows in Table 3.

Table 3 − Test Structures C1 through C4 Design Rules

	C1	***C2***	***C3***	***C4***
Outer layer pad size	27 mil	27 mil	27 mil	27 mil
Inner layer antipad size	25 mil	28 mil	33 mil	38 mil
Drilled hole size (DHS)	14.5 mil	14.5 mil	14.5 mil	14.5 mil
Antipad diameter minus DHS	10.5 mil	13.5 mil	18.5 mil	23.5 mil
Via edge to inner layer antipad edge (assuming optimal registration)	5.25 mil	6.75 mil	9.25 mil	11.75 mil
Bias pins	13 to 17	14 to 17	15 to 17	16 to 17

Test Structures D1 and D2

The two "D" test structures have alternating parallel plates from layer 1 to layer 10. All even layers are connected to one electrode and all odd layers are connected to the other electrode. The electrode plates on each layer are the same size and lie directly over one another. The design of the D1 and D2 test structure is the same. This structure is useful to evaluate the layer to layer dielectric resistance to temperature, humidity, and bias of materials.



A conceptual representation of the "D" test structure is shown to the upper right. Design details on each of the two "D" test structures follows in Table 4.

Table 4 − Test Structures D1 and D2 Design Rules

	D1	***D2***
Electrode Size	1.65 x 3.55 inch	1.65 x 3.55 inch
Bias pins	19 to 21	20 to 21

Factors Thought to Effect CAF

Following below is a listing of factors that are believed to affect PCB fab life under CAF testing. When building boards with this test board if is

Process:	Drilled hole roughness
	Hole clean process (chemistry used, dwell time, amount of etchback, etc.)
	Ionic residue from layer fab, hole clean, and metallization processes
	Drilled hole to inner layer registration
Materials:	Reinforcement type (Electrical glass, aramid fiber, paper, etc.)
	Adhesion treatment used on electrical glass
	Resin type (FR4, BT, Polyimide, Cyanate Ester, PPO, PPE, etc.)
	Copper tooth profile
Design:	Layer to layer dielectric thickness
	Via edge to via edge spacing
	Via location (in or out of line with the reinforcement weave direction)
	Via edge to antipad clearance edge spacing, i.e., keepout space
	Hole size and board thickness, i.e., drill wander on small diameter drill bits
Environmental:	Temperature
	Relative humidity
	Bias (AC, DC, voltage...)

Data Provided for CAF TV1

This xxx−yyyy−02−01_readme_061500 file in .pdf format

The xxx−yyyy−02−01.zip file which contains all other files which are listed below:

File	***Description***
xxx−yyyy−02.pdf	Fab drawing
xxx−yyyy−02−01_contents.txt	Text file on formats used, files included, conventions used, where to get help...
used_aps.txt	Text file list apertures used
01_top.art	Layer 1 gerber file
02_PLANE.art	Layer 2 gerber file
03_PLANE.art	Layer 3 gerber file
04_PLANE.art	Layer 4 gerber file
05_PLANE.art	Layer 5 gerber file
06_PLANE.art	Layer 6 gerber file
07_PLANE.art	Layer 7 gerber file
08_PLANE.art	Layer 8 gerber file
09_PLANE.art	Layer 9 gerber file
10_bot.art	Layer 10 gerber file
50_masktop.art	Layer 1 solder mask gerber file
51_maskbot.art	Layer 10 solder mask gerber file
outline.art	Board outline gerber file
ncdrill1.tap	NC drill data
ncdrill2.tap	NC drill data

Contact Information

For further information on the CAF TV1 contact:

Michael Freda
Sun Microsystems, Inc.
901 San Antonio Road, UMPK15−103
Palo Alto, CA 94303−4900
650−786−6385 direct
650−786−6457 fax
michael.freda@eng.sun.com

Karl Sauter
Sun Microsystems, Inc.
901 San Antonio Road, UMPK15−103
Palo Alto, CA 94303−4900
650−786−7663 direct
650−786−6457
karl.sauter@eng.sun.com

References

1. J.P Mitchell and T.L. Welsher, "Conductive Anodic Filament Growth in Printed Circuit Materials", Printed Circuit World Convention II (June, 1981).
2. J.N. Lahti, R.H. Delaney and J.N. Hines, "The Characteristic Wearout Process in Epoxy−Glass Printed Circuits for High Density Electronic Packaging", 17th Annual Proceedings Reliability Physics 1979, pp. 39−43, (April 24−26, 1979).
3. D.J. Lando, J.P Mitchell and T.L. Welsher, "Conductive Anodic Filaments in Polymeric Dielectrics: Formation and Prevention", 17th Annual Proceedings Reliability Physics 1979, pp. 51−63, (April 24−26, 1979).

Revision History

Part Number	***Comment***
270−4921−01−01	Initial release by Sun Microsystems, Inc.
xxx−yyyy−02−01	Released to the IPC